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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,738	06/25/2003	Mutsuko Hatano	HITA.0407	9854

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,738	HATANO ET AL.	
	Examin r	Art Unit	
	Stanetta D. Isaac	2812	AU

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 04/07/04 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on the patent application serial number 10/602,738 was filed after the mailing date of the office action on 04/07/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Hara et al. Patent Application Publication US 2002/0031876.

5. Hara discloses the semiconductor method as claimed. See FIGS. 1A-37, where Hara teaches a method for fabricating an image display device comprising an active matrix substrate having a pixel region formed with a large number of pixels arranged as an matrix and a drive circuit region formed with an active circuit for supplying a drive signal to said pixels from outside said pixel region, the method comprising the steps of:

Step 1) "forming a polycrystalline silicon film over said pixel region and said drive circuit region of said active matrix substrate;"(pertaining to claims 1-4)

As stated on page 4, paragraph [0077], the "amorphous silicon (a-Si film)" is irradiated and scanned by "excimer laser" "to form large-size polysilicon crystals," which confirms "forming a polycrystalline silicon film".

In addition, as stated on page 12, paragraph [0244], "the initial film is a p-Si film formed through...by solid phase growth..." which also confirms, "forming a polycrystalline silicon film"

Finally, as stated on page 1, paragraph [0013], the semiconductor device contains a "pixel region" and a "peripheral circuit region" (implied "drive circuit region") that by "crystallizing a semiconductor film... into active semiconductor films" confirms, "forming a polycrystalline silicon film over said pixel region and said drive circuit region of said active matrix substrate"

Step 2) "selectively irradiating a portion of the polycrystalline silicon film located in said drive circuit region with a laser beam having a pulse width and/or a pulse interval modulated by scanning the laser beam or the substrate to form discrete reformed regions each composed of a quasi-strip-like-crystal silicon film resulting from reformation, said quasi-strip-like-crystal

silicon film having a crystal boundary continuous in the direction scanning;" (pertaining to claims 1-4)

See figures 16A-16D, where an illustration of the selective irradiation is performed, and as stated on page 4, paragraphs [0077-0080] and page 7, paragraphs [0128-0132], where "...two parallel thin-line patterns" are formed on the semiconductor film for the purpose of "selectively irradiating a portion of the polycrystalline silicon film..."

In addition, the semiconductor film, for example, "amorphous silicon" is formed in an "ribbon or island shape" that is crystallized by the use of an "excimer laser" "to form large-size polysilicon crystals." Furthermore, the semiconductor film is "...crystallized again by laser heating."

It is inherent that an "quasi-strip-like-crystal silicon film resulting from reformation" would be formed, since the amorphous silicon film is irradiated and scanned by the "excimer laser" to form "polysilicon crystals" and then "fused and crystallized again by the laser heating" confirms that "quasi-strip-like-crystal silicon film" is formed.

Step 3) "and forming the active circuit such that a carrier moving direction coincides with a direction of said crystal boundary in each of said discrete reformed regions." (Pertaining to claims 1-4)

As stated on page 7, paragraph [0132], "a TFT using an active semiconductor film prepared in this manner...the characteristics are improved... " Shows, "that a carrier moving direction coincides with a direction of said crystal boundary in each of said discrete reformed regions."

6. Pertaining to claims 2-4, Hara teaches the method of claim 1, comprising an active matrix substrate having a pixel region formed with a large number of pixels arranged as a matrix and a drive circuit region formed with an active circuit for supplying a drive signal to said pixels from outside said pixel region, the method comprising the steps of:

Step 4) "and forming the active circuit such that a carrier moving direction coincides with a direction of said crystal reformation, said wherein each of said discrete reformed regions, said step of forming a polycrystalline silicon film comprises the substeps of forming an amorphous silicon film and reforming said amorphous silicon film into a polycrystalline silicon film." Please see figures and statements provided in Step 2)

7. Pertaining to claim 5, Hara teaches the method of claim 1, wherein the irradiation with said laser beam having the pulse width and/or pulse interval modulated is performed intermittently at specified intervals to form, into a generally rectangular configuration, each of individual reformed regions composing each of said discrete reformed regions. Please see figures and statements provided in Step 2). In addition, see page 5, paragraph [0085] pertaining to the shapes of the laser beam.

8. Pertaining to claims 6 and 7, Hara teaches the method of claim 5, wherein the irradiation (scanning) with said laser beam having the pulse width and/or pulse interval modulated is performed intermittently along one of the peripheral sides of the active matrix substrate to arrange the individual reformed regions composing each of said discrete reformed regions at specified intervals in a direction which said drive circuit region extends. Please see statements provided in Steps 1) and 2)

9. Pertaining to claim 8, Hara teaches the method of claim 5, wherein the scanning with said laser beam having the pulse width and/or pulse interval modulated is performed along each of opposing two of the peripheral sides of the active matrix substrate to arrange the individual reformed regions composing each of said discrete reformed regions formed along each of the two sides at specified intervals in a direction in which said drive circuit region disposed along each of the two sides extends. Please see statements provided in Steps 1) and 2)

10. Pertaining claim 9, Hara teaches the method of claim 5, wherein the scanning with said laser beam having the pulse width and/or pulse interval modulated is performed along one of the sides of the active side adjacent to said one side reformed regions composing each of said discrete reformed regions at specified intervals in direction in which said drive circuit region disposed along said one side extends and in a direction in which said drive circuit region disposed along extends. Please see statements provided in Steps 1) and 2)

11. Pertaining to claim 10, Hara teaches the method of claim 5, wherein the scanning with said laser beam having the pulse width and/or pulse interval modulated performed along each of opposing two of the sides of the active matrix substrate and along a side adjacent to each of said two sides to arrange the individual reformed regions composing each of said discrete reformed regions at specified intervals in a direction in which said drive circuit disposed along the adjacent side extends. Please see statements provided in Steps 1) and 2)

12. Pertaining to claim 11, Hara teaches the method of claim 5, wherein said plurality of discrete reformed regions are divided into blocks and said blocks are arranged in two or more rows parallel with each other in a direction in which said drive circuit region extends.

13. Pertaining to claim 12, Hara teaches the method of claim 11, wherein the individual reformed regions composing each of the discrete reformed regions that have been divided into blocks are arranged in two or more rows parallel with each other in a direction in which said drive circuit region extends. Please statements provided in Step 2)

14. Pertaining to claim 13, Hara teaches the method of claim 11, wherein said blocks of said discrete reformed regions are arranged in two or more rows parallel to each other in mutually staggered relation in a direction which said drive circuit region extends. Please statements provided in Step 2)

15. Pertaining to claim 14, Hara teaches the method of claim 13, wherein the individual reformed regions composing each of the discrete reformed regions that have been divided into blocks are arranged in two or more rows parallel with each other in mutually staggered relation in a direction in which said drive region extends. Please statements provided in Step 2)

16. Pertaining to claim 16, Hara teaches the method of claim 1, wherein the positioning mark on said active matrix substrate is formed preliminarily on said active matrix substrate or on an underlie for the amorphous silicon film or the polycrystalline silicon film on the active matrix substrate.

17. See figures 14 and 27, and as stated on page 6, paragraph [0115-0016], page 10, paragraph [0201], Hara teaches the uses of "position markers **31**" and "positioning markers **75**"

18. Pertaining to claim 17, Hara teaches the method of claim 1, further comprising the step of: Step 6) "forming the positioning mark on the amorphous silicon film or the polycrystalline silicon film on said active matrix substrate through irradiation with said laser having the pulse width and/or the pulse interval modulated."

19. See figures 14 and 27, and as stated on page 6, paragraph [0115-0016], page 10, paragraph [0201], Hara teaches the uses of "position markers **31**" and "positioning markers **75**"

20. Pertaining to claim 18, Hara teaches the method of claim 1, further comprising the step of: Step 7) "forming a thin-film transistor in said active circuit." Please see provided in Step 3)

21. Pertaining to claim 19, Hara teaches the method of claim 1, further comprising at least the steps of: Step 8) "bonding, to said active matrix substrate, color filter substrate disposed in opposing relation thereto at specified distance therefrom;

Step 9) "and sealing a liquid crystal a space between said active matrix substrate and said color filter substrate.

22. Pertaining to claim 20, Hara teaches the method of claim 1 , further comprising at least the steps of: Step 10) "forming an organic EL layer for each of the pixels composing said pixel region of said active matrix substrate;"

Step 11) "and bonding a protective substrate to said active matrix said organic EL of said active matrix substrate is covered therewith.

Pertaining to the above claims see page 11, paragraph [0216], it is inherent that Hara teaches these limitations because the prior art of record is specifically drawn to manufacturing "high-quality liquid crystal display device with its drive circuit being incorporated"

23. Pertaining to claim 21, Hara teaches "the method of claim 1, wherein said laser beam is a solid-state laser having a wavelength of 200 nm to 1200 nm." See page 4, paragraph [0083], where the solid-state laser is disclosed.

24. Pertaining to claim 22, Hara teaches "the method of claim 1, wherein an irradiation width of said laser beam is 20 μm to 1000 μm." See page 6, paragraph [0121], where the laser beam is disclosed.

25. Pertaining to claim 23, Hara teaches "the method of claim 1, wherein a. scanning speed of said laser beam or a scanning speed of said substrate is 50 mm/s to 3000 mm/s." See page 6, paragraph [0121], where the laser beam or scanning speed is disclosed.

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al Patent Application Publication US 2002/0031876 in view of Stanley Wolf and Richard N. Tauber *Silicon Processing for the VLSI Era Volume I-Process Technology.*

28. Hara discloses the semiconductor method as claimed. See FIGS. 1A-37, where Hara teaches a method for fabricating an image display device comprising an active matrix substrate having a pixel region formed with a large number of pixels arranged as an matrix and a drive circuit region formed with an active circuit for supplying a drive signal to said pixels from outside said pixel region, the method comprising the steps of:

Step 1) "forming a polycrystalline silicon film over said pixel region and said drive circuit region of said active matrix substrate;"(pertaining to claims 1-4)

As stated on page 4, paragraph [0077], the "amorphous silicon (a-Si film)" is irradiated and scanned by "excimer laser" "to form large-size polysilicon crystals" which confirms "forming a polycrystalline silicon film".

In addition, as stated on page 12, paragraph [0244], "the initial film is a p-Si film formed through...by solid phase growth..." which also confirms, "forming a polycrystalline silicon film"

Finally, as stated on page 1, paragraph [0013], the semiconductor device contains a "pixel region" and a "peripheral circuit region" (implied "drive circuit region") that by "crystallizing a semiconductor film... into active semiconductor films" confirms, "forming a polycrystalline silicon film over said pixel region and said drive circuit region of said active matrix substrate"

Step 2) "selectively irradiating a portion of the polycrystalline silicon film located in said drive circuit region with a laser beam having a pulse width and/or a pulse interval modulated by scanning the laser beam or the substrate to form discrete reformed regions each composed of a quasi-strip-like-crystal silicon film resulting from reformation, said quasi-strip-like-crystal silicon film having a crystal boundary continuous in the direction scanning;" (pertaining to claims 1-4)

See figures 16A-16D, where an illustration of the selective irradiation is performed, and as stated on page 4, paragraphs [0077-0080] and page 7, paragraphs [0128-0132], where "...two parallel thin-line patterns" are formed on the semiconductor film for the purpose of "selectively irradiating a portion of the polycrystalline silicon film..."

In addition, the semiconductor film, for example, "amorphous silicon" is formed in an "ribbon or island shape" that is crystallized by the use of an "excimer laser" "to form large-size

polysilicon crystals." Furthermore, the semiconductor film is "...crystallized again by laser heating."

It is inherent that an "quasi-strip-like-crystal silicon film resulting from reformation" would be formed, since the amorphous silicon film is irradiated and scanned by the "excimer laser" to form "polysilicon crystals" and then "fused and crystallized again by the laser heating" confirms that "quasi-strip-like-crystal silicon film" is formed.

Step 3) "and forming the active circuit such that a carrier moving direction coincides with a direction of said crystal boundary in each of said discrete reformed regions." (pertaining to claims 1-4)

As stated on page 7, paragraph [0132], "a TFT using an active semiconductor film prepared in this manner...the characteristics are improved... " shows, "that a carrier moving direction coincides with a direction of said crystal boundary in each of said discrete reformed regions."

29. However, pertaining to claim 15, Hara fails the method of claim 1, further comprising the step "forming, by a photolithographic technique, positioning mark on the amorphous silicon film or the polycrystalline silicon film on said active matrix substrate."

30. See figure 1 and pages 407-408, under *BASIC PHOTORESIST TERMINOLOGY*, where Wolf teaches that a SiO_2 film is being etched by photolithographic techniques. In view of Wolf, it would have been obvious to one of ordinary skill in the art to incorporate the photolithographic techniques since Hara teaches that the "parallel thin-line patterns" are formed of a silicon oxide material where conventional art teaches that silicon oxide can be etched by using this technique.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 14, 2004

John F. Niebling
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